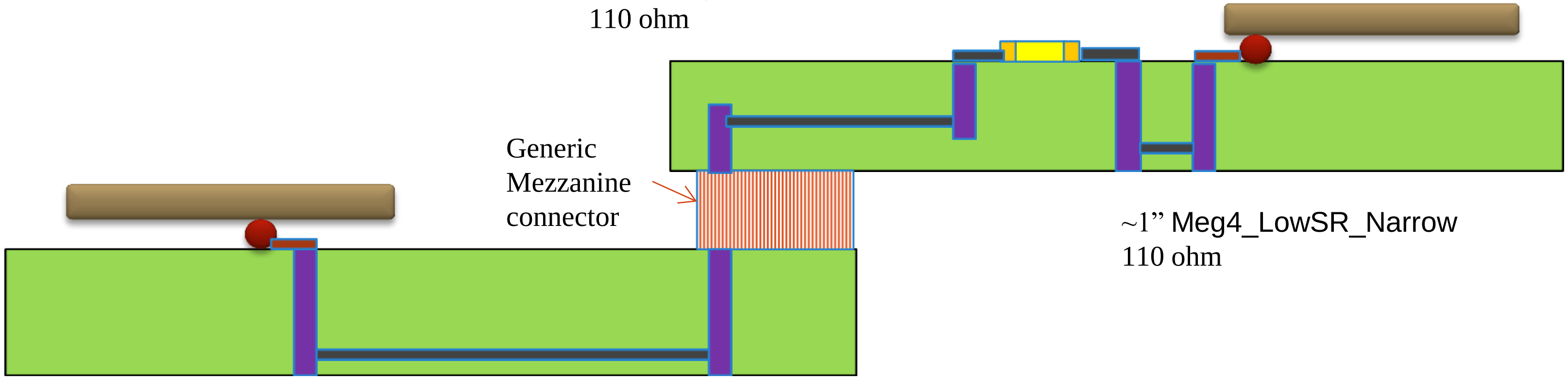
Topology Description
CAUI-4 Main Mezzanine Design and Back Drilled (13.4 dB)

Richard Mellitz
Intel Corporation

09/24/2013

CAUI-4 Mezzanine Topology back drilled

18 mil stubs



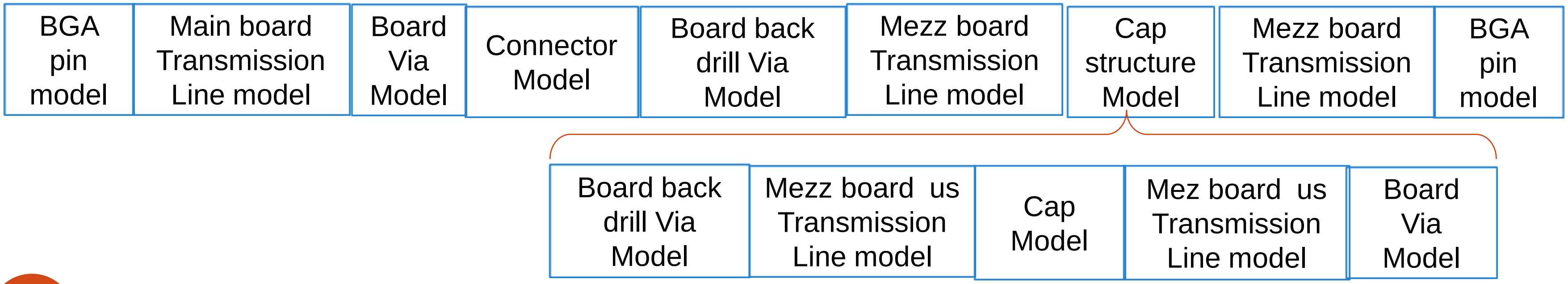
~0.25, 0.25 ” Meg4_LowSR_Narrow_ms
90 ohm

~6,5” Meg4_LowSR_Narrow_ms
110 ohm

Generic
Mezzanine
connector

~1” Meg4_LowSR_Narrow
110 ohm

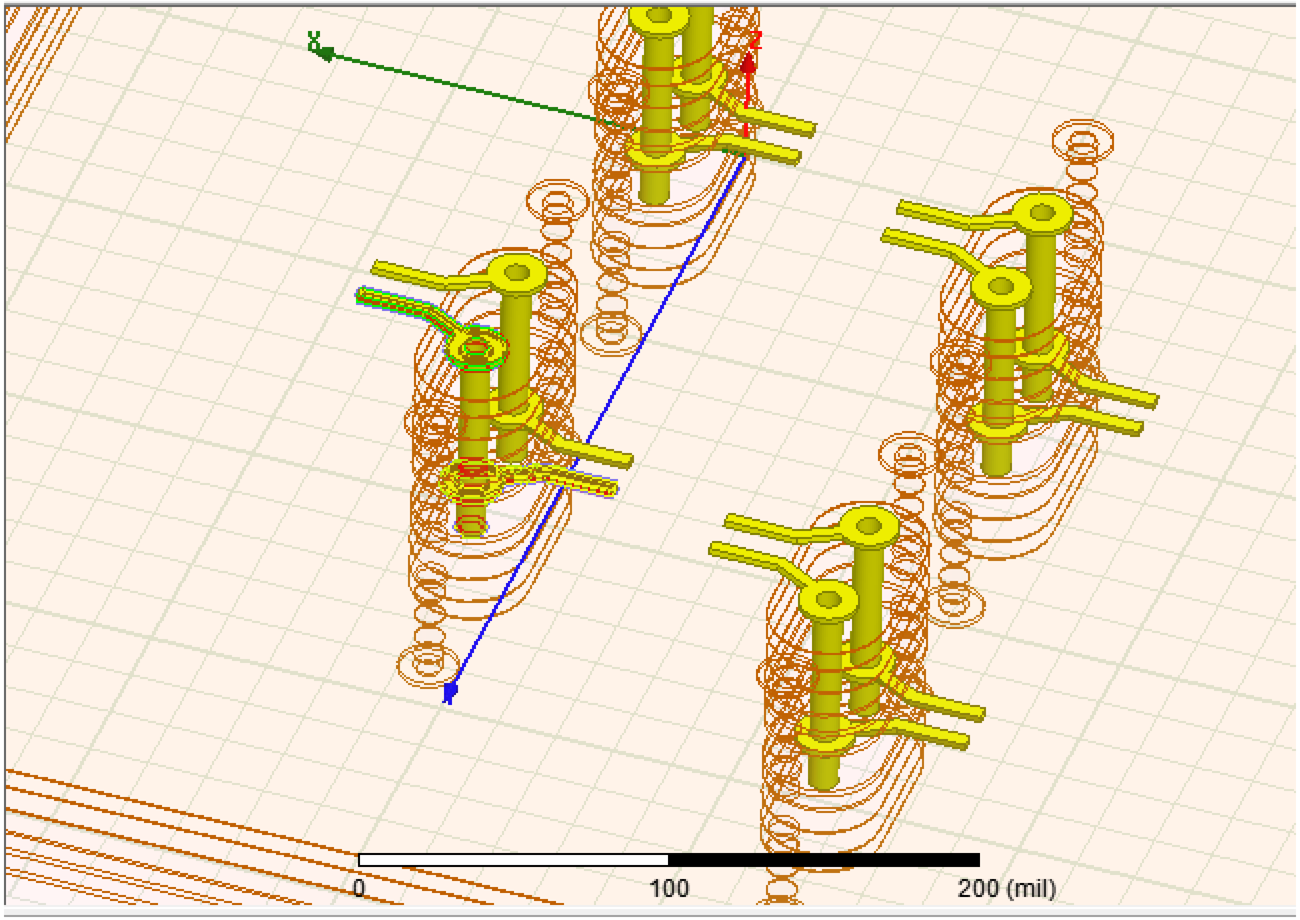
~4” Meg4_LowSR_Narrow
90 ohm



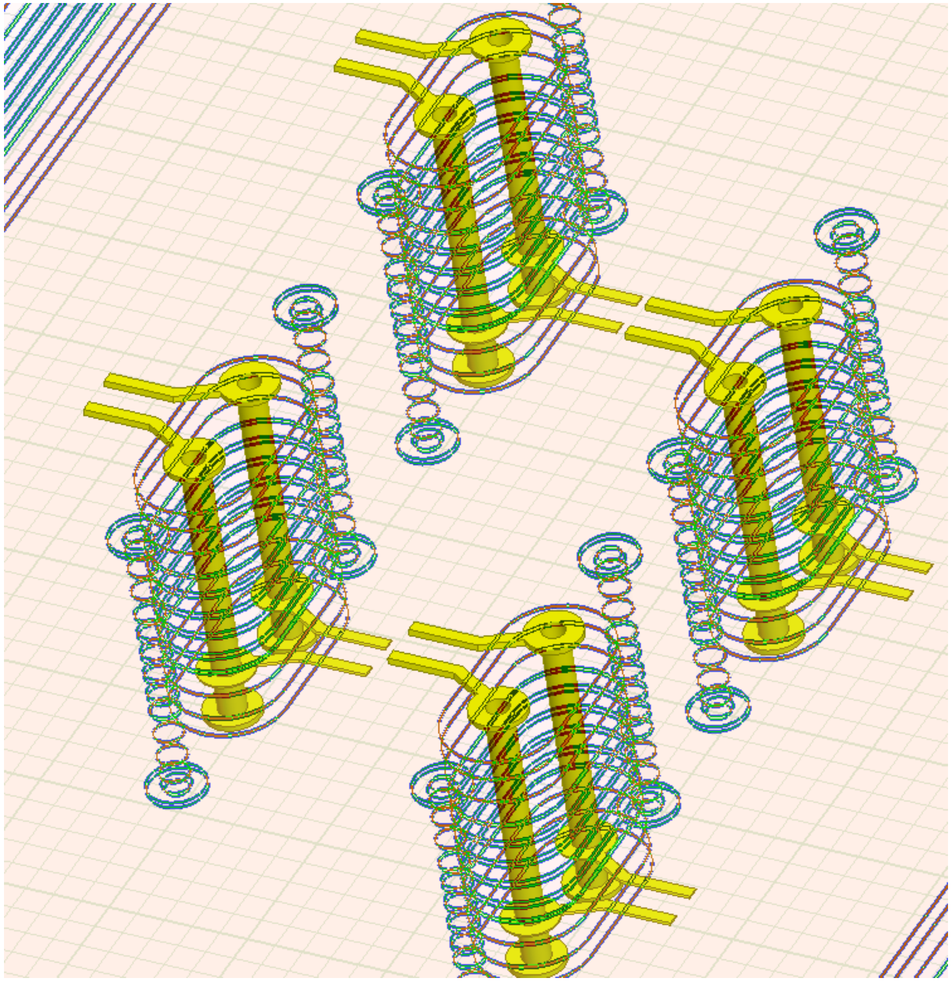
BGA pin model | Main board Transmission Line model | Board Via Model | Connector Model | Board back drill Via Model | Mezz board Transmission Line model | Cap structure Model | Mezz board Transmission Line model | BGA pin model

Board back drill Via Model | Mezz board us Transmission Line model | Cap Model | Mez board us Transmission Line model | Board Via Model

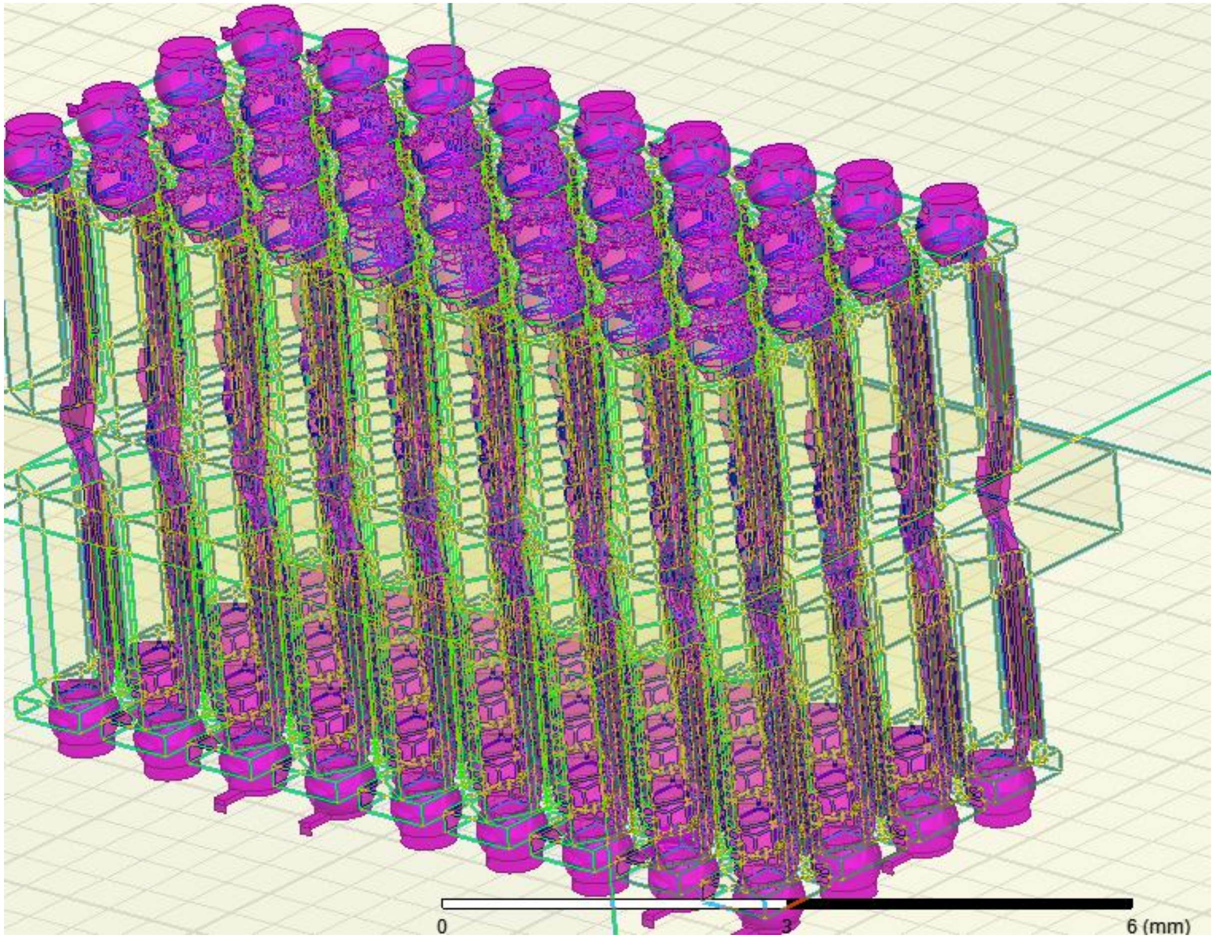
Stubbed / back drilled Via Model - 12 layer stack up 18 mil stub



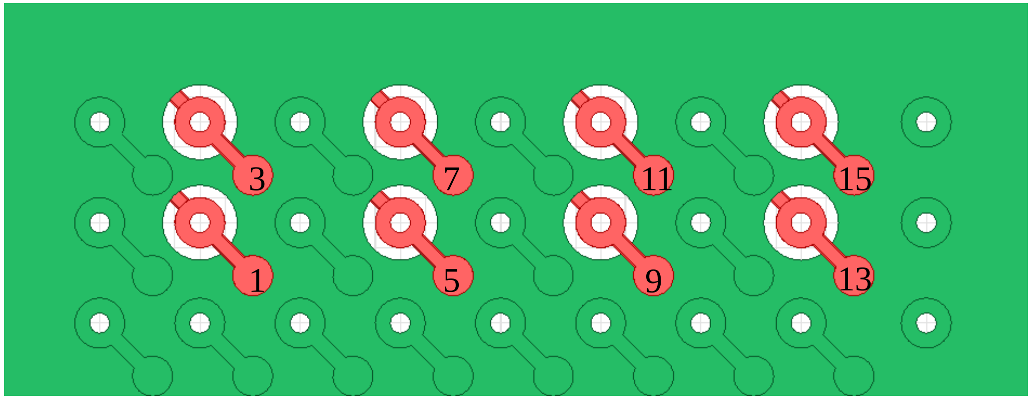
Stubbed Via Model -
12 layer stack up 18 mil stub

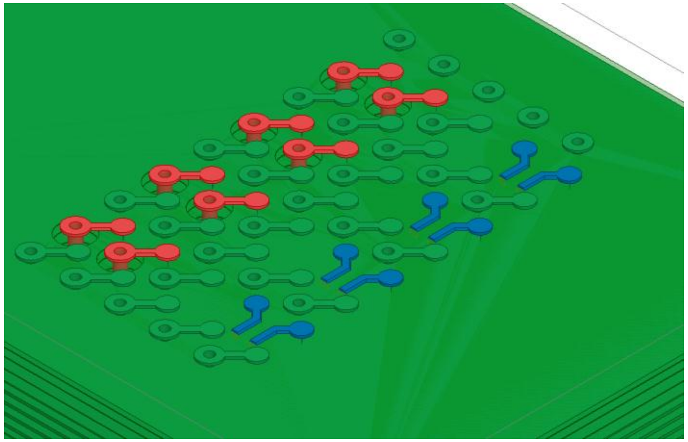


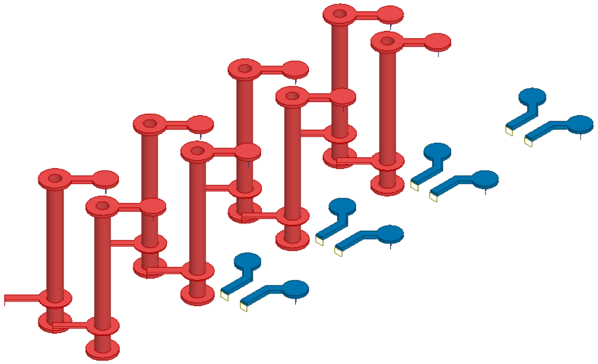
Mezzanine Connector Model

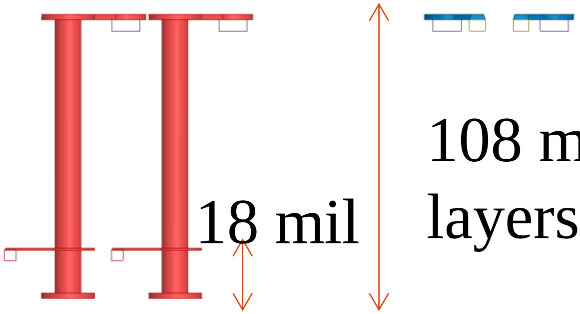


BGA Attach Model









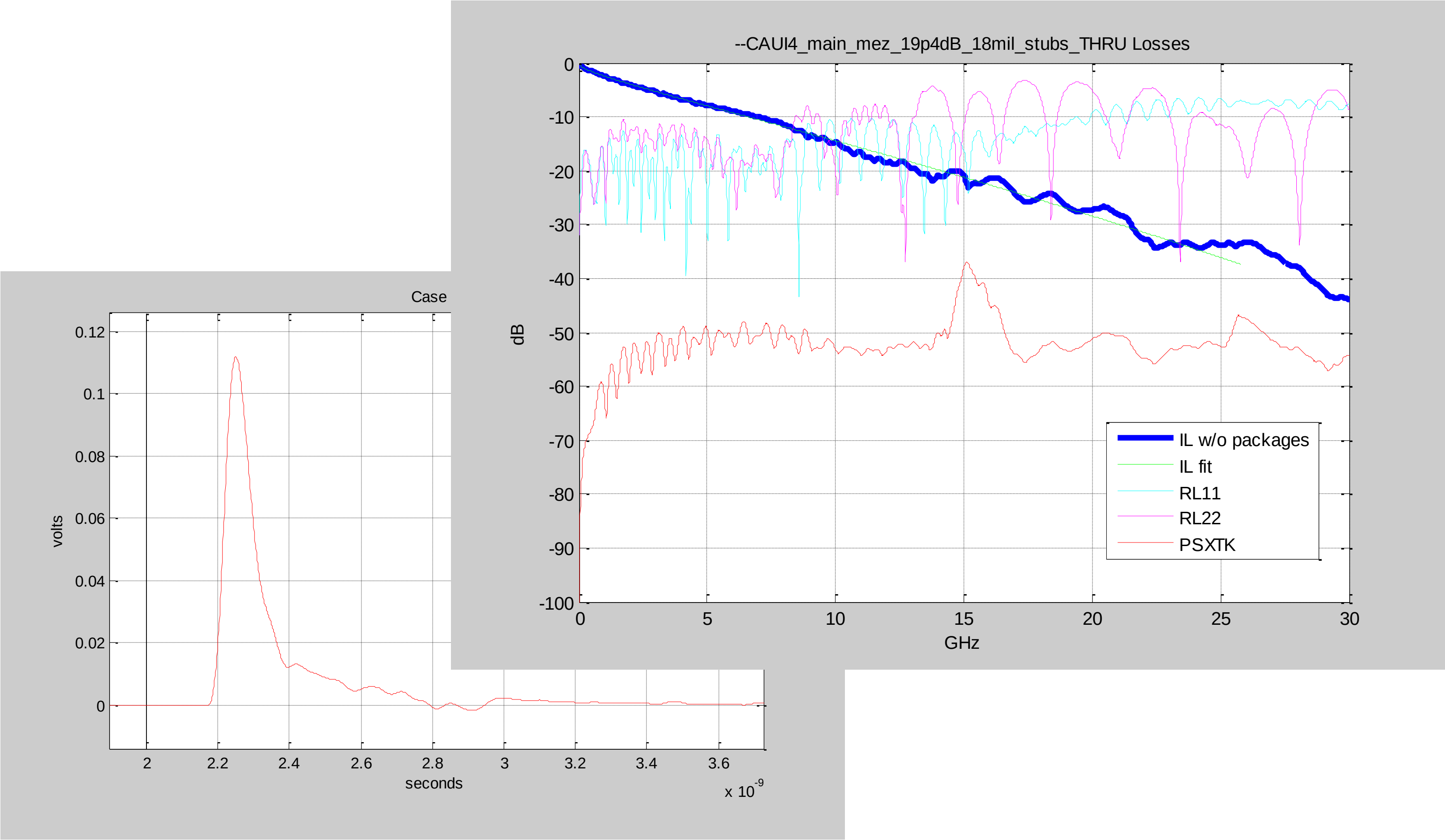
18 mil

108 mil (12 layers)

Transmission line models

	Z0 (ohms)	Loss dB/in @12.9GHz	Finished Trace Width (mils)	
Meg4_LowSR_Narrow	90.00	-1.341	3.71	
Meg4_LowSR_Narrow	110.03	-1.267	3.31	
Meg4_LowSR_Narrow_ms	90.01	-0.867	6.21	

Differential IL and RL Responses and SBR w 12 mm Package



4th order Bessel Thomson Rx filter applied